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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,804	03/03/2004	Takashi Takamura	118577	4351

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EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,804	TAKAMURA, TAKASHI	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 23 May 2005.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed May23, 2005 has been entered; no new claims have been introduced.

Priority

2. Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d) prior to declaration of an interference, a translation of the foreign application should be submitted under 37 CFR 1.55 in reply to this action.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Konishi et al. ("Konishi") US PG-Pub 2004/0235261.

Konishi discloses (figs. 1-3 and 8 and pars. 0016-0019) a solid-state imaging device, comprising: a pixel array having a plurality of pixels 10A arranged in a matrix; and a control unit 157 (par. 0075) that controls the pixel array; each of the pixels including: a photo diode 11 that generates carriers depending on an intensity of incident light; an accumulation region 17 that accumulates the generated carriers; an insulated-gate output transistor 12 that outputs a signal

according to a threshold voltage that changes depending on a number of the carriers accumulated in the accumulation region; and an insulated-gate clear transistor 13a that discharges, during a discharging period, the carriers accumulated in the accumulation region and that discharges during an accumulation period, spilled carriers that exceed a capacity of the accumulation region.

5. Claim 2 is rejected under 35 U.S.C. 102(e) as being anticipated by Konishi.

Konishi discloses (figs. 1-3 and 8 and pars. 0016-0019) a solid-state imaging device, comprising: a pixel array having a plurality of pixels 10A arranged in a matrix; and a control unit 157 (par. 0075) that controls the pixel array; each of the pixels including: a photo diode 11 that generates carriers depending on an intensity of incident light; an accumulation region 17 that accumulates the generated carriers; an insulated-gate output transistor 12 that outputs a signal according to a threshold voltage that changes depending on a number of the carriers accumulated in the accumulation region; and an insulated-gate clear transistor 13a that discharges the carriers accumulated in the accumulation region; the clear transistor including a substrate region that is formed below the gate electrode of the clear transistor; and the substrate region comprising: an upper region 15 that is formed in a vicinity of the gate electrode of the clear transistor and that has a relatively low impurity concentration; and a lower region 18 that is formed below the upper region and that has a relatively high impurity concentration.

6. Claim 3-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Konishi.

Konishi discloses (figs. 1-3 and 8 and pars. 0016-0019) a solid-state imaging device, comprising: a pixel array having a plurality of pixels 10A arranged in a matrix; and a control unit 157 (par. 0075) that controls the pixel array; each of the pixels including: a photo diode 11 that

generates carriers depending on an intensity of incident light; an accumulation region 17 that accumulates the generated carriers; an insulated-gate output transistor 12 that outputs a signal according to a threshold voltage that changes depending on a number of the carriers accumulated in the accumulation region; and an insulated-gate clear transistor 13a that discharges the carriers accumulated in the accumulation region; each of the pixels further comprising: a pixel-forming region 15 of a second conductivity type that is formed on a semiconductor substrate 14 of a first conductivity type and where at least one of the pixels is formed; a buried region of a first conductivity type that is formed in the pixel-forming region and that includes a first partial buried region 19 and a second partial buried region 17, the first partial buried region formed at a relatively deep position and having a relatively low impurity concentration, the second partial buried region formed at a relatively shallow position and having a relatively high impurity concentration, the second partial buried region being the accumulation region; and a discharging region (par. 0079) of a first conductivity type that is formed in the pixel-forming region and into which carriers discharged from the accumulation region flow; the output transistor including an output a gate electrode 22 and being formed above the pixel-forming region on the accumulation region with an insulating film 21 therebetween; and the clear transistor including the gate electrode 13a that is formed above the pixel-forming region between the buried region and the discharging region.

Regarding claim 4, Konishi discloses the photo diode including a junction region between the first partial buried region 19 and the pixel-forming region 15.

Regarding claim 5, Konishi discloses both the accumulation region 17 and the buried region 16 functioning as a source region of the clear transistor.

Regarding claim 6, Konishi discloses the first gate electrode 22 having a substantially annular shape; and the output transistor including a source region 23 that is formed inside the first gate electrode and a drain region 24 that is formed outside the first gate electrode.

Regarding claim 7, Konishi discloses the first conductivity type being a p-type; the second conductivity type being an n-type; and the carriers being holes.

As for the operational limitations of the control unit and the clear transistor recited in claims 1-3, claims directed to an apparatus must distinguish from the prior art in terms of structure rather than function, In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also In re Swinehart, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971; In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over US PG-Pub 2001/0011736 in view of Shizukuishi USPN 6,781,178.

Dierickx discloses in figs. 2 and 14 a solid-state imaging device, comprising: a pixel array having a plurality of pixels (par. 0035) arranged in a matrix; and a control unit (par. 0114) that controls the pixel array; each of the pixels including: a photo diode (par. 0063) that generates carriers depending on an intensity of incident light; an accumulation region 3 that accumulates the generated carriers; an insulated-gate output transistor 7'/ 7 that outputs a signal

according to a threshold voltage that changes depending on a number of the carriers accumulated in the accumulation region; and an insulated-gate clear transistor (par. 0073) that discharges the carriers accumulated in the accumulation region, but lacks anticipation of an insulated-gate clear transistor that discharges, during a discharging period, the carriers accumulated in the accumulation region and that discharges during an accumulation period, spilled carriers that exceed a capacity of the accumulation region.

Shizukuishi discloses in figs. 1-4 a solid-state imaging device, comprising: a pixel array having a plurality of pixels arranged in a matrix; and an insulated-gate clear transistor WM that discharges, during a discharging period, the carriers accumulated in the accumulation region and that discharges during an accumulation period, spilled carriers that exceed a capacity of the accumulation region (col. 9, lines 51-62).

Since Dierickx and Shizukuishi are both from the same field of endeavor, solid-state imaging devices, Shizukuishi's teachings would have been recognized in the pertinent art of Miida. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate an insulated-gate clear transistor with Dierickx's device, since that would improve sensitivity and response speed as taught by Shizukuishi.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dierickx US PG- in view of Shizukuishi.

Dierickx discloses in figs. 2 and 14 a solid-state imaging device, comprising: a pixel array having a plurality of pixels (par. 0035) arranged in a matrix; and a control unit (par. 0114) that controls the pixel array; each of the pixels including: a photo diode (par. 0063) that generates carriers depending on an intensity of incident light; an accumulation region 3 that

accumulates the generated carriers; an insulated-gate output transistor 7'/ 7 that outputs a signal according to a threshold voltage that changes depending on a number of the carriers accumulated in the accumulation region; and an insulated-gate clear transistor (par. 0073) that discharges the carriers accumulated in the accumulation region, but lacks anticipation of an insulated-gate clear transistor that discharges spilled carriers in order to prevent carriers from entering the accumulation region.

Shizukuishi discloses in figs. 1-4 a solid-state imaging device, comprising: a pixel array having a plurality of pixels arranged in a matrix; and an insulated-gate clear transistor that discharges spilled carriers in order to prevent carriers from entering the accumulation region (col. 9, lines 51-62); and the substrate region comprising: an upper region 23 (horizontal portion of layer 23) that is formed in a vicinity of the gate electrode of the clear transistor and that has a relatively low impurity concentration; and a lower region 25 that is formed below the upper region and that has a relatively high impurity concentration.

Since Dierickx and Shizukuishi are both from the same field of endeavor, solid-state imaging devices, Shizukuishi's teachings would have been recognized in the pertinent art of Miida. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate an insulated-gate clear transistor with Dierickx's device, since that would improve sensitivity and response speed as taught by Shizukuishi.

10. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miida US PG-Pub 2002/016703 in view of Shizukuishi.

Miida discloses in figs. 1-8 a solid-state imaging device, comprising: a pixel array having a plurality of pixels (par. 0085) arranged in a matrix; and a control unit (par. 0095) that controls

the pixel array; each of the pixels including: a photo diode 111 that generates carriers depending on an intensity of incident light; an accumulation region 25 that accumulates the generated carriers; an insulated-gate output transistor 112 that outputs a signal according to a threshold voltage that changes depending on a number of the carriers accumulated in the accumulation region, but lacks anticipation of an insulated-gate clear transistor that discharges, during a discharging period, the carriers accumulated in the accumulation region and that discharges during an accumulation period, spilled carriers that exceed a capacity of the accumulation region.

Shizukuishi discloses in figs. 1-4 a solid-state imaging device, comprising: a pixel array having a plurality of pixels arranged in a matrix; and an insulated-gate clear transistor WM that discharges, during a discharging period, the carriers accumulated in the accumulation region and that discharges during an accumulation period, spilled carriers that exceed a capacity of the accumulation region (col. 9, lines 51-62).

Since Miida and Shizukuishi are both from the same field of endeavor, solid-state imaging devices, Shizukuishi's teachings would have been recognized in the pertinent art of Miida. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate an insulated-gate clear transistor with Miida's device, since that would improve sensitivity and response speed as taught by Shizukuishi.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
August 2, 2005

EVAN PERT
PRIMARY EXAMINER